REMARKS

The Examiner is thanked for his careful and very thorough Office Action.

Claims 1-4 have been rejected.

Note that the amendment to Claim 4 is intended simply to correct a typo in the dependency.

The amendments to Claims 1 and 3 are also not intended to be substantive. They are being amended for clarification purposes to preclude an interpretation of the claims which apparently was being followed by the Examiner. In view of this interpretation, the claims are being amended to more clearly distinguish the present invention from the *Baldwin* patent.

Claims 5-40 have been added. Support for the claims is essentially the same as that for Claims 1-4, but the added claims are directed to methods and systems according to the disclosure of the application as filed. The support for Claims 6, 8, 12, 16, 20, 24, 28, 32, 36, and 40 can be found in Fig. 1A. These new claims are respectfully asserted not to introduce new matter, and their entry is respectfully requested.

The foregoing amendments to the specification are submitted to improve clarity, and to remove various typographical and other minor informalities. These changes are respectfully asserted not to introduce new matter, and their entry is respectfully requested.

Art Rejections

The art rejections are all respectfully traversed.

Review of the References

Baldwin relates to a graphics processing chip which uses a deep pipeline of multiple asynchronous units, separated by FIFO's, to achieve a high net throughput in 3D rendering. Besides the output interface to the frame buffer, a separate interface is to a local buffer which can be used for data manipulation.[1] Each read or write returns a single pixel 32 to 48 bits wide.[2] The local buffer can only store non-displayable pixel information.[3] This patent does not disclose a memory interface which provides a high bandwidth interface independent of the serial message-passing interface directly to a memory that is capable of storing displayable pixel information.

Manze et al. relates to an image data value storage system.

If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out very specifically where such teaching may be found.

Rejections Under 35 USC 102(b)

Claims 1 and 3 stand rejected as being anticipated by Baldwin.

Amended Claim 1 now recites "**a memory interface which provides a high bandwidth interface independent of said serial message-passing interface directly to a**

[1] Col. 4, *ll.* 38-43.
[2] Col. 7, *ll.* 52-53; col. 22 *ll.* 62-63.
[3] Col. 7, *ll.* 1-4.

memory associated with said graphics accelerator, said memory capable of storing displayable pixel information."

The Examiner has suggested that the high bandwidth interface to memory disclosed by the present application is found in *Baldwin*. However, the interface to the local buffer memory disclosed in *Baldwin* is not high bandwidth. A typical localbuffer configuration would be 48 bits per pixel[4], and the local buffer memory cannot be used to store displayable pixel information.[5] Instead, displayable pixel information must be stored in the frame buffer memory which is typically separate from the local buffer memory.[6] Therefore, two separate memories are actually used in the *Baldwin* architecture.

The present application discloses a memory that is 256 bits wide physically, and with DDR memory, it appears to be 512 bits wide. Each access now returns sufficient data for multiple pixels. Optimizing high bandwidth with a memory architecture where memory is organized in tiles allows the architecture to accesses multiple byte-sized tiles of pixels simultaneously and not one pixel at a time. Having this architecture gives the present invention real and technical advantages. As stated in the present application:

> **...[T]he present architecture transmits pixel data through a different high-bandwidth bus path, which provides for much greater**

---

[4] Col. 22 *ll.* 62-63.
[5] Col. 7, *ll.* 1-4.
[6] Col. 6, *ll.* 64-67.

overall fill rate. The combination of message-passing control architecture with extremely high-bandwidth to memory provides a further improvement over the GLINT architecture[7]...

Some observations contrasting this architecture to earlier ones of 3Dlabs:

The message stream does not visit every unit.

Trying to route a linear message stream though the texture pipes is fairly problematic, although fanning it out like in Gamma 3 would have been an option.

It turns out that the texture units in the texture pipe have little or no state or any need for the color and coordinate information, but are heavily pipelined or have deep latency FIFOs. Not forcing the message stream to be routed through them saves on pipeline register and FIFO widths.

[7] Paragraph [0032].

The only down side is in testing as the interfaces are not so uniform across units.

The message stream does not carry any pixel data except for upload/download data and fragment coverage data.

The private data paths give more bandwidth and can be tailored to the specific needs of the sending and receiving units.

The private data path between the Shading Unit (via the Texture Mux Unit) and Pixel Unit doesn't need to go through the Router, or any other unit. If the message stream were increased in width to give the required bandwidth then the cost would be borne in a number of places. It will be necessary to have it FIFO buffered, particularly when the Router places the texture subsystem first so that texture processing is not stalled while waiting for the Pixel Unit to use its data, but this cannot

> **happen until the Tile message has reached it. Having one FIFO doing this buffering will be a lot cheaper than a distributed one and will ease chip layout routing.**
>
> **The message stream is still the only mechanism for loading registers and synchronizing internal operations.**[8]

Of course, this text in the specification does not define the scope or interpretation of any of the claims, which speak for themselves. *Baldwin* does not disclose such a memory interface or the corresponding advantages.

Claim 3 has also been amended to recite "**a high bandwidth memory interface independent of said serial message-passing interface which interfaces to a memory of said graphics accelerator, said memory capable of storing displayable pixel information.**"

Applicant respectfully submits that the amended claims are now more patentably distinct from *Baldwin*. Therefore, Applicant respectfully requests withdrawal of this rejection.

[8] Paragraphs [0079-0087].

Rejections Under 35 USC 103(a)

Claims 2 and 4 stand rejected as being unpatentable over *Baldwin* in view of *Manze et al.*

Dependent Claims 2 and 4 depend directly from independent Claims 1 and 3 and incorporate all the limitations thereof. For this reason, Applicant respectfully requests withdrawal of this rejection.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Robert Groover for an interview to resolve any remaining issues.

Respectfully submitted,

N. Elizabeth Pham, Reg.No. 49,042

Customer Number 29106

Attorney for Applicant

11330 Valley Dale Drive, Dallas TX 75230

214-363-3038 *groover@technopatents.com* December 21, 2003